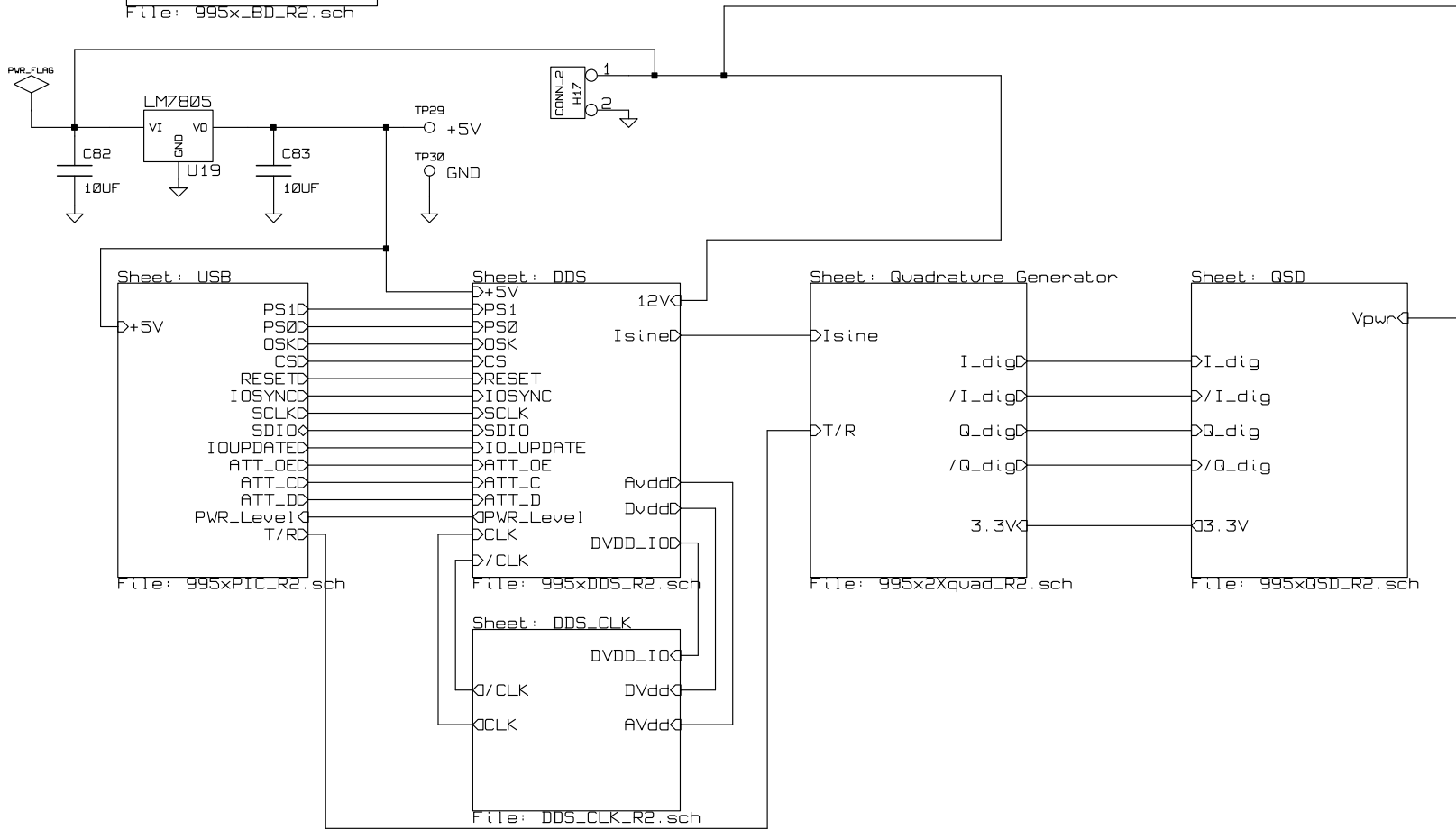


Sheet: Block Diagram

File: 995x_BD_R2.sch



Sheet: USB
 +5V
 PS1D
 PS0D
 OSKD
 CS
 RESETD
 IOSYNCD
 SCLKD
 SDIOD
 IOUPDATED
 ATT_OED
 ATT_CD
 ATT_DD
 PWR_LevelD
 T/RD
 File: 995xPIC_R2.sch

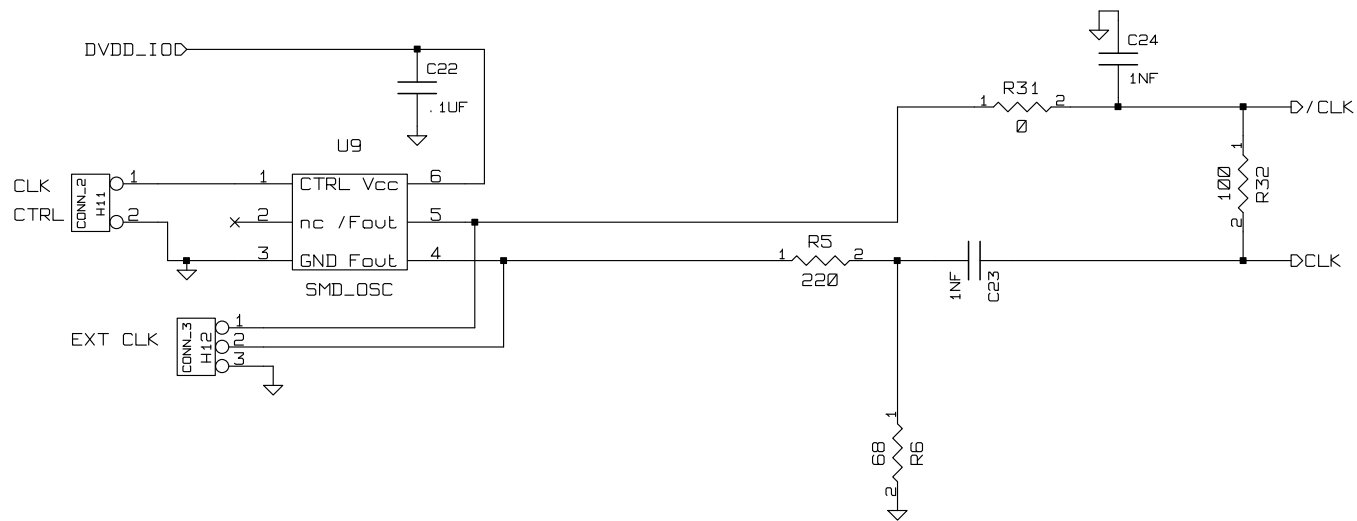
Sheet: DDS
 +5V
 PS1
 PS0
 OSK
 CS
 DRESET
 DIOSYNC
 SCLK
 SDIO
 IO_UPDATE
 ATT_OE
 ATT_C
 ATT_D
 PWR_Level
 CLK
 /CLK
 12V
 IsineD
 AvddD
 DvddD
 DVDD_I0D
 File: 995xDDS_R2.sch

Sheet: DDS_CLK
 DVDD_I0
 DVdd
 AVdd
 D/CLK
 OCLK
 File: DDS_CLK_R2.sch

Sheet: Quadrature Generator
 T/R
 I_digD
 /I_digD
 Q_digD
 /Q_digD
 3.3V
 File: 995x2Xquad_R2.sch

Sheet: QSD
 VpwrD
 I_dig
 /I_dig
 Q_dig
 /Q_dig
 3.3V
 File: 995xQSD_R2.sch

Designed by David A. Brainerd		
Bluebird Originals		
Title: AD995x Root Sheet		
Size: A	Date: 2 nov 2008	Rev:
KiCad E.D.A. EESchema (2007-11-29-c)		Sheet: 1/7



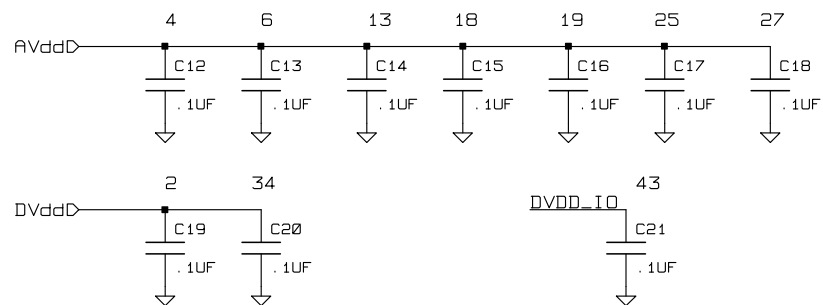
CLOCK OPTIONS:

CMDS OSC: Put 1nF from /CLK to GND., Omit R31,R32

The 220 and 68 ohm resistors are for a 3.3V clock. Change as required for other amplitudes.

LVDS OSC Replace R5 with 0ohm, delete R6, Replace C23 with 0ohm, delete C24

EXT OSC: Omit SMD_OSC (or disable from pin 1), If single-ended put 1nF from /CLK to GND, adjust 220 and 68 for proper amplitude. Omit R31.



DDS Chip Power Bypass Caps

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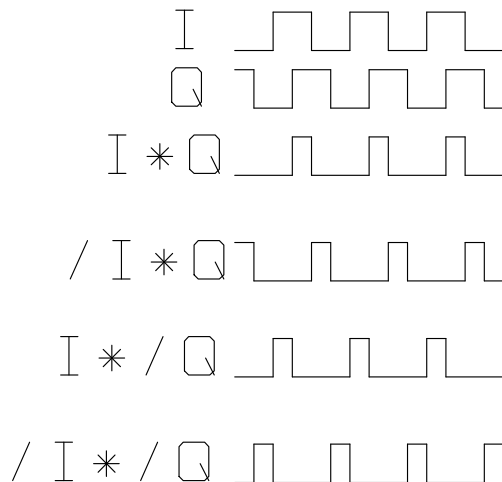
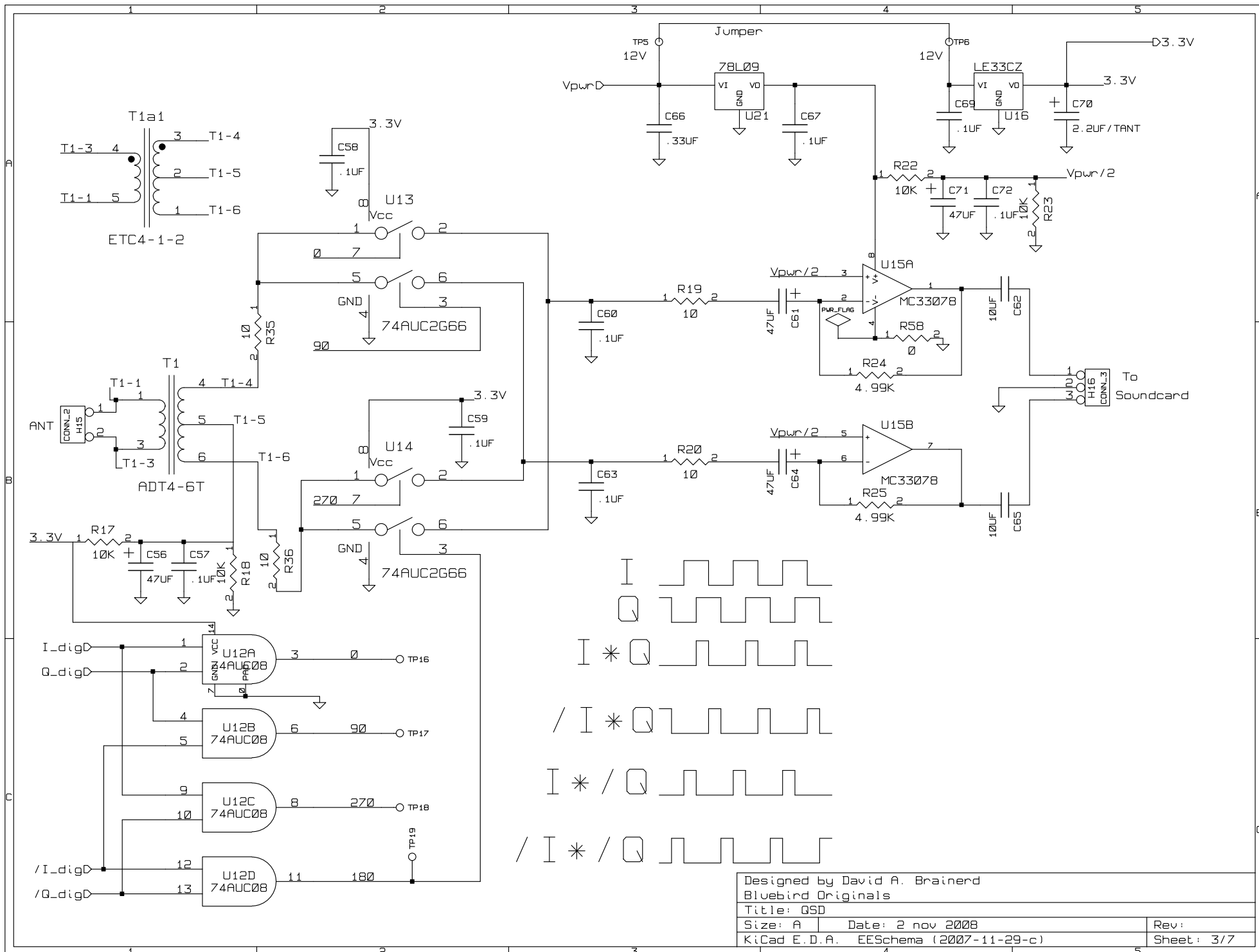
Title: DDS Clock Circuit

Size: A Date: 2 nov 2008

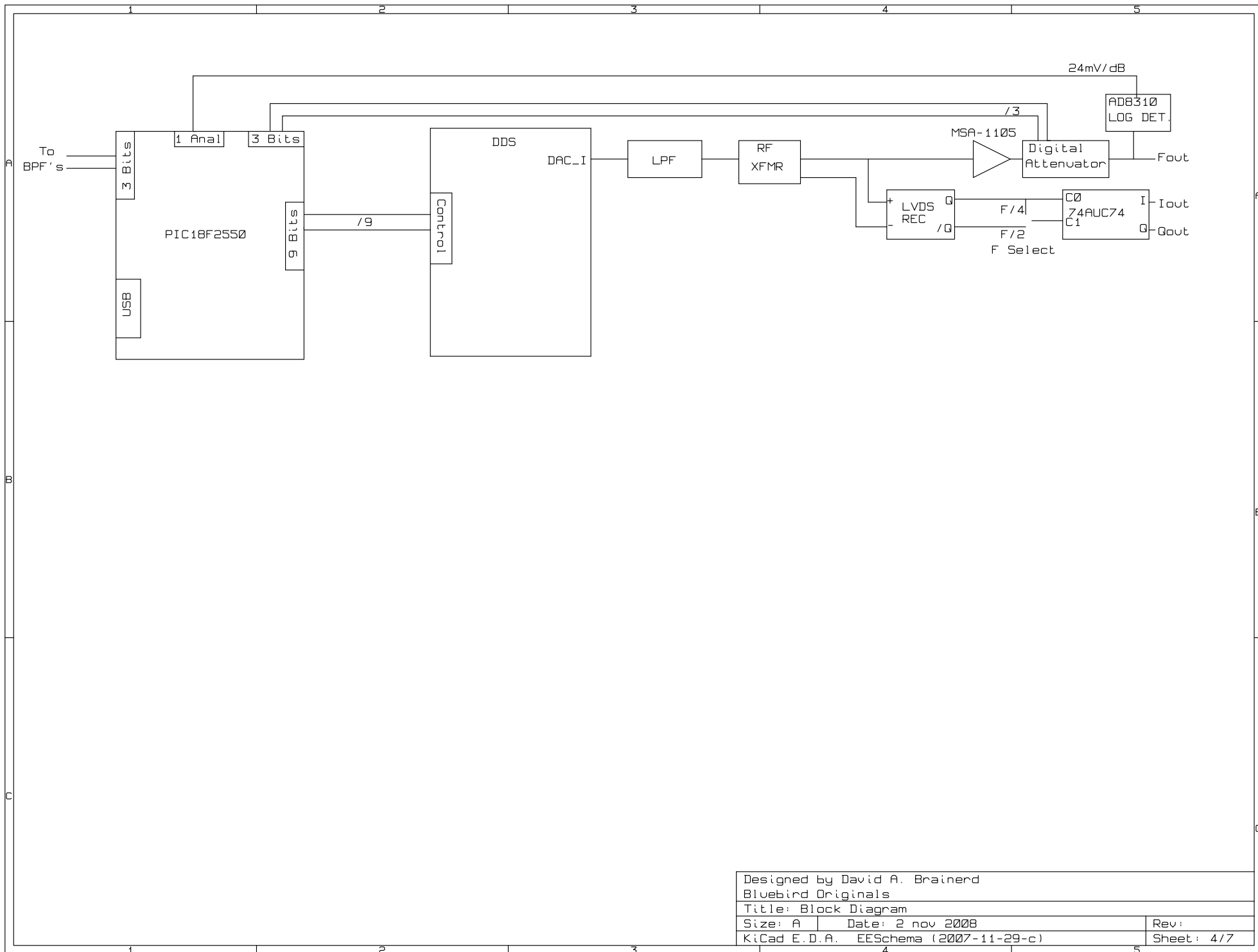
KiCad E.D.A. EESchema (2007-11-29-c)

Rev:

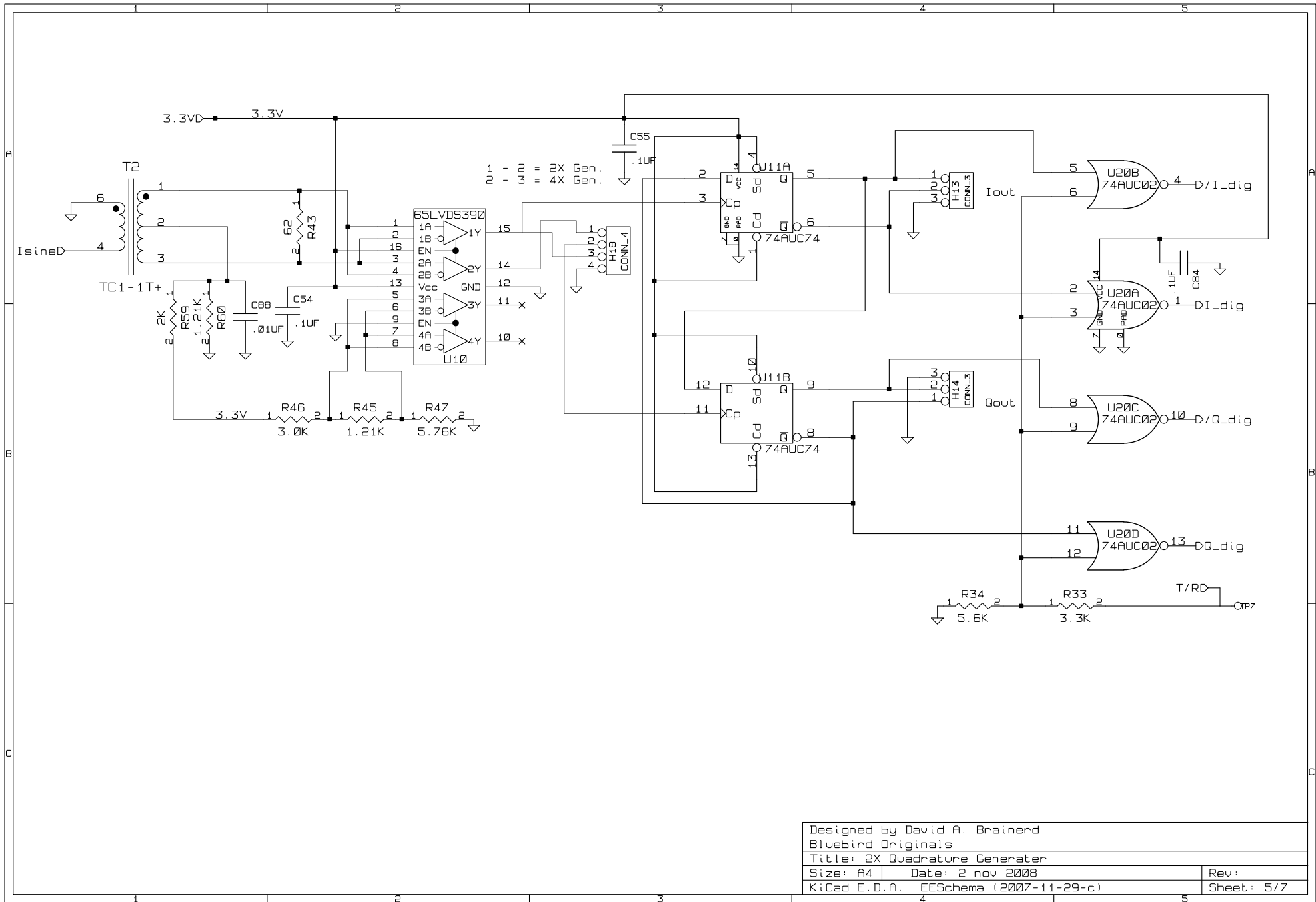
Sheet: 2/7

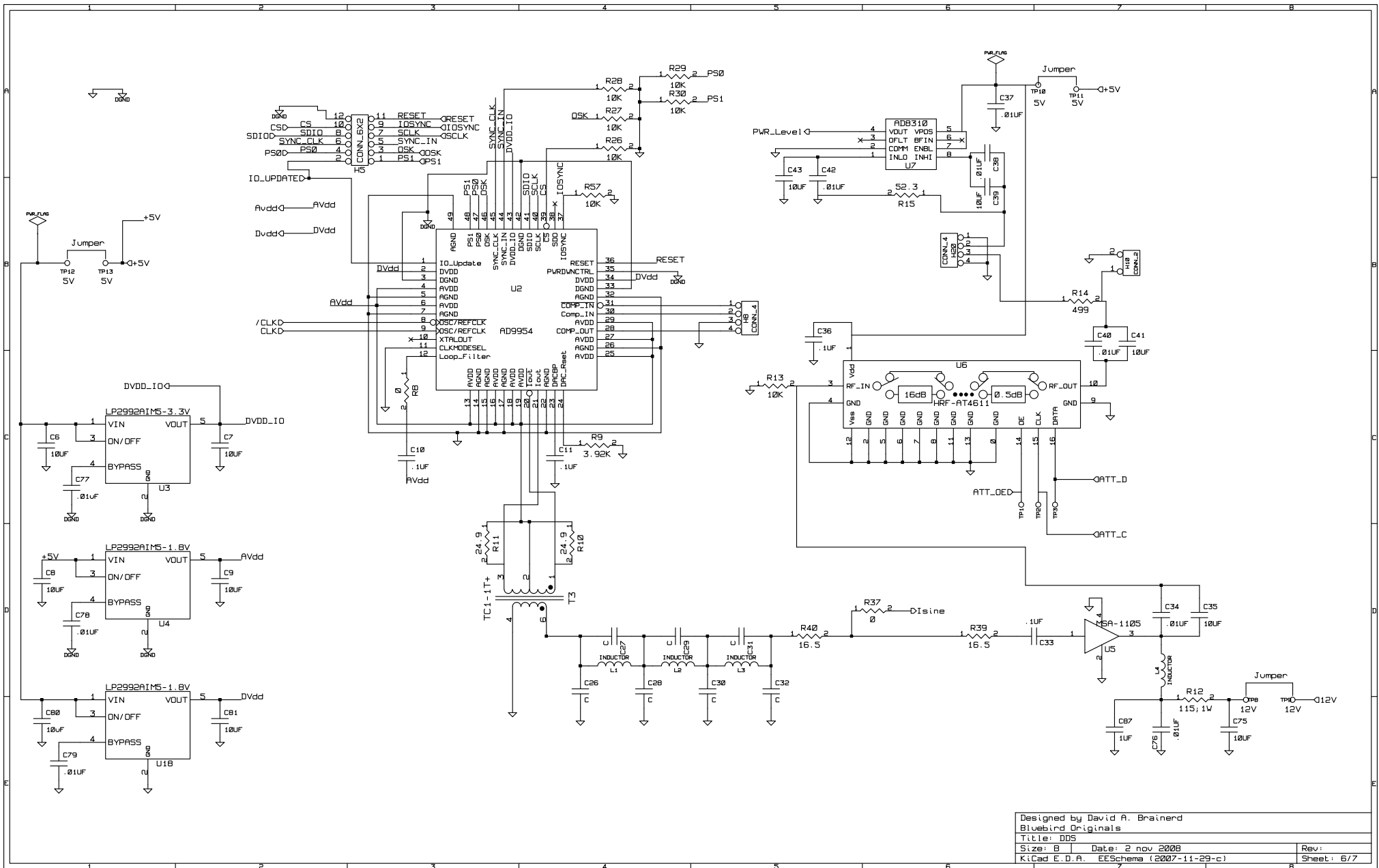


Designed by David A. Brainerd
 Bluebird Originals
 Title: QSD
 Size: A Date: 2 nov 2008 Rev:
 KiCad E.D.A. EESchema (2007-11-29-c) Sheet: 3/7

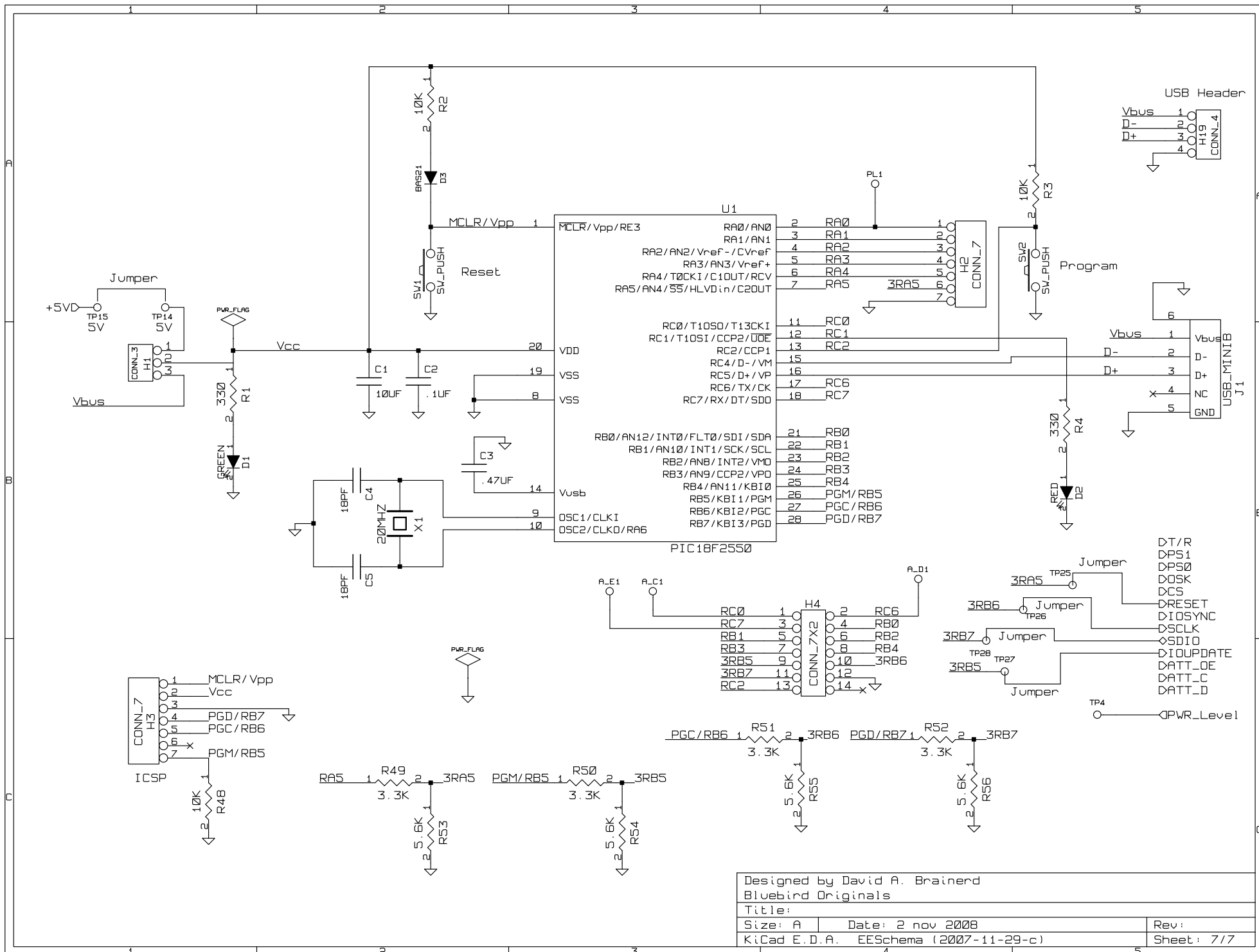


Designed by David A. Brainerd		
Bluebird Originals		
Title: Block Diagram		
Size: A	Date: 2 nov 2008	Rev:
KiCad E.D.A. EESchema (2007-11-29-c)		Sheet: 4/7





Designed by David A. Brainerd
 Bluebird Originals
 Title: DDS
 Size: B Date: 2 nov 2008 Rev:
 KiCad E.D.A. EESchema (2007-11-29-c) Sheet: 6/7



Designed by David A. Brainerd
 Bluebird Originals
 Title:
 Size: A Date: 2 nov 2008 Rev:
 KiCad E.D.A. EESchema (2007-11-29-c) Sheet: 7/7